Unit 1: Components of a Computer
(1a. Components and Performance of Processors, AS Content)

Marks: /44

Answer **all** the questions.

1. A processor contains a number of special registers.

Name and describe **three** buses used to convey information between the special registers.

1

2

3

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[6]

2. A processor contains a number of special registers.

Explain the need for the following registers.

(i) Program Counter (PC)

---[2]

(ii) Memory Address Register (MAR)

---[2]

(iii) Memory Data Register (MDR)

---[2]

3. Computer architectures use registers including the accumulator.

Describe **two** ways in which the accumulator is used.

1

2

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[4]

4. A processor uses a number of different registers. One of these is the Current Instruction Register.

Describe the use of special registers and their functions during the fetch-decode-execute cycle, including jump instructions, reading from and writing to memory.

The quality of written communication will be assessed in your answer to this question.

[8]

5(a). A company is designing a new low-power processor to be used in a smartwatch.

The processor contains a control unit.

Describe the role of the control unit in the processor.

[2]

(b). The processor fetches data from memory location 50.

Explain how the following are used in the process:

Memory Address Register

Address Bus

Data Bus

Memory Data Register

[4]

6. Describe how each of these improves a processor's performance:

(i) fast clock speed

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[2]

(ii) large cache memory

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[2]

7. An example of a register in the Von Neumann Architecture is the Accumulator (ACC).

Give a Little Man Computer instruction that will copy the contents of the accumulator into memory when executed.

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[1]

8. 

A student, Dan, on a limited budget finds his computer is running slowly. He uses his computer for university work and internet browsing.

Discuss what measures can be taken to improve Dan's computer's performance. You should explain what these measures are, why they improve the performance and justify whether you would recommend them.

--- [9]

END OF QUESTION PAPER

Question			Answer/Indicative content	Marks	Guidance
1			• Control bus… • …transmits control signals from the control unit (to other parts of the processor) • Data bus… • …carries the data (from one place to another) • Address bus… • …carries the location address (register) where the data is going (to or from)	6	These are the expected responses as they are the buses listed in the specification, however, other responses are acceptable, for example named buses like 'EIDE, a local bus' and 'Video bus to maintain screen display'. Serial and parallel buses are not acceptable because they are not named. Not a memory bus. Control bus does not send program instructions. Examples would include interrupt signals / read / write operation carried out Examiner's Comments Understanding of the purpose of the three bus types named in the specification continues to improve although there is still the desire among candidates to imbuethem with rather more power than they have got. Typical is the desire to say that the bus 'stores' something rather than acting as a conduit. On a base level candidates can picture data being sent around the processor in the data bus and the details of where it is being sent to are carried in the address bus. The control bus simply passes the control signals to the registers from the control unit.
			Total	6	
2		i	–Is needed to store the address of the next instruction (to be processed) –Value is then sent to the MAR –After sending the value the PC is incremented / changed to address held in CIR if the operation is a Jump	2	Examiner's Comments Few candidates gained full marks for this question. Some candidates demonstrating confusion between which registers hold the actual instruction/data and which hold the memory location address of the instruction/data.
		ii	– Contains the address of the instruction (to be accessed in memory)… – …address of instruction sent from PC – Contains the address of the data (to be accessed in memory)… – …address of data sent from CIR	2	Examiner's Comments Again, some candidates demonstrated confusion between registers. A common error was 'address of next instruction'.

Question			Answer/Indicative content	Marks	Guidance
		iii	– Contains the instruction which has been accessed from memory – Contains the data which has been accessed from memory – That is referenced by the MAR / Instruction sent to CIR – acts as a buffer	2	**Examiner's Comments** Although most candidates did state that this register holds data/instructions there was a lack of clarity about where the data/instruction was coming from/going to, hence not clearly explaining the need for the register.
			Total	**6**	
3			• Temporary storage • for data being processed / during calculations • I/O in processor… • … used as a buffer / gateway	4	**Examiner's Comments** A good discriminator question, with candidates achieving a range of marks.
			Total	**4**	

Question			Answer/Indicative content	Marks	Guidance
4			**Mark band 6-8. High level response.** Candidate has given a comprehensive response stating **most** of the bullets for all three points and has used appropriate technical language throughout their answer. There are few, if any, spelling or grammatical errors. **Mark band 3-5. Medium level response.** Candidate has given an adequate response stating **some** of the bullets for all three points or has explained two comprehensively. The candidate has used some appropriate technical language in their answer. There may be a few spelling or grammatical errors. **Mark band 0-2. Low level response.** Candidate has given an adequate response stating some of the bullets for two points or has explained one comprehensively. The candidate may have used some appropriate technical language in their answer. There are some spelling or grammatical errors. • Registers ◦ Mentions CIR MDR MAR PC and ACC ◦ Jump instruction CIR sends **address** to PC ◦ PC incremented ◦ MDR **copies** data to CIR ◦ CIR holds the data to be decoded.. ◦ …into opcode and operand • Saving ◦ CIR sends address to MAR.. ◦ …sends data to MDR ◦ All data to be saved uses the ACC • Other relevant points ◦ All arithmetic and logical operations use the ACC ◦ Mention of buses (Address Data or Control) ◦ Control unit for synchronisation ◦ Mention of Interrupt Register ◦ ALU performs calculations	8	accept: Memory Buffer Register **Examiner's Comments** As was expected for the banded response question all candidates could write something about the registers and almost all of those could write something about a jump instruction. There were some good write-ups about the use of the accumulator and the ALU, some mentioned the use of buses, but Control Unit and Interrupt register were a rare find. Saving was a bit patchy with some rather vague descriptions although there were still the occasional gems to be found. A good spread of responses overall.
			Total	**8**	

Question			Answer/Indicative content	Marks	Guidance
5	a		Two from: □ Decodes instructions. [1] □ Sends control signals to coordinate movement of data through the processor / execute instruction. [1] □Controls buses [1]	2	Accept manages / coordinates / synchronises the FDE cycle for BP 1 and 2 Examiner's Comments Some candidates answered this question well, however descriptions in some cases lacked attention to detail with some responses not going beyond '…the control unit tells all the parts of the processor what to do…' which is not creditworthy at this level.
	b		□ Stores the memory location of the data to be fetched/ stores the memory location 50 [1] □ Transfers the memory location to access the data (to be fetched)/ transfers the memory location 50 [1] □ Transfers the data from the memory location specified by MAR / Transfers the data from the memory location 50 [1] □ Stores the data from memory location specified by MAR / Stores the data from memory location 50 [1]	4	Examiner's Comments Candidates were required in this question to relate their explanations to the scenario. Many candidates did this and therefore scored well on this question.
			Total	6	

Question			Answer/Indicative content	Marks	Guidance
6		i	• Gives more cycles per second • More instructions can be executed per second • So the program takes less time to run *(1 per -, Max 2)*	2	Do not accept '…data is processed quickly…' as BP3 **Examiner's Comments** Many candidates achieved some credit on this question but candidates did not achieve full marks due to lack of attention to detail in their description. Many candidates used phrases such as 'processor will run quicker / faster' without describing how a fast clock speed would enable this.
		ii	• More space for data / instructions in cache memory • RAM needs to be accessed less frequently • Accessing cache is quicker than accessing the RAM *(1 per -, Max 2)*	2	**Examiner's Comments** Similarly, the lack of detailed responses limited credit achieved on this question. Many candidates used phrases such as 'large cache means faster processing' without describing how a large cache would enable this.
			Total	**4**	
7			-STA	1 AO1.1	Accept STO **Examiner's Comment** Well answered in the main, demonstrating an improvement in candidate understanding of LMC instruction set.
			Total	**1**	

Question			Answer/Indicative content	Marks	Guidance
8			**Mark Band 3 – High Level** **(7–9 marks)** The candidate demonstrates a thorough knowledge and understanding of a wide range of ways a computer's performance can be improved and justifies how these measures improve performance; the material is generally accurate and detailed. The candidate is able to apply their knowledge and understanding directly and consistently to the context provided. Evidence / examples will be explicitly relevant to the explanation. The candidate provides a thorough discussion which is well-balanced. Evaluative comments are consistently relevant and well-considered. *There is a well-developed line of reasoning which is clear and logically structured. The information presented is relevant and substantiated.* **Mark Band 2 – Mid Level** **(4–6 marks)** The candidate demonstrates reasonable knowledge and understanding of a range of methods of improving a computer's performance and justifies how many of these improve performance; the material is generally accurate but at times underdeveloped. The candidate is able to apply their knowledge and understanding directly to the context provided although one or two opportunities are missed. Evidence / examples are for the most part implicitly relevant to the explanation. The candidate provides a reasonable discussion, the majority of which is focused. Evaluative comments are for the most part appropriate, although one or two opportunities for development are missed. *There is a line of reasoning presented with some structure. The information presented is in the most part relevant and supported by some evidence.*	9 AO1.1 (2) AO1.2 (2) AO2.1 (2) AO3.3 (3)	**AO1: Knowledge and Understanding** The following is indicative of possible factors/evidence that candidates may refer to but is not prescriptive or exhaustive: Methods of improving performance - Replace CPU with faster CPU - Add more/Faster RAM - Add a graphics card - Upgrade to faster secondary storage - Update OS - Install a lighter weight OS - Defragment the hard disk - Check for viruses and spyware. **AO2.1: Application** The selected knowledge/examples should be directly related to the specific question. The example below is not prescriptive or exhaustive: - A newer CPU may have a faster clock speed and so execute more instructions per second. It may have multiple cores and so be able to execute several programs simultaneously (or one in parallel). It may have more cache meaning comparatively slower RAM can be accessed less frequently. - More RAM means more programs can be open simultaneously without the need to use much slower virtual memory.

Question			Answer/Indicative content	Marks	Guidance
			Mark Band 1 – Low Level **(1–3 marks)** The candidate demonstrates a basic knowledge of how a computer's performance can be improved. Limited understanding is shown of how these measures improve performance; the material is basic and contains some inaccuracies. The candidate makes a limited attempt to apply acquired knowledge and understanding to the context provided. The candidate provides a limited discussion which is narrow in focus. Judgments if made are weak and unsubstantiated. *The information is basic and communicated in an unstructured way. The information is supported by limited evidence and the relationship to the evidence may not be clear.* **0 marks** No attempt to answer the question or response is not worthy of credit.		- Adding a graphics card will speed up the rendering of 3D graphics as GPU has specialist instructions and can apply the same instruction to multiple pieces of data simultaneously. - The slower the secondary storage the longer it takes to load files/program/data. A faster secondary storage device can improve this. May choose to use flash memory (i.e. SSD) - OS makers often release updates and some of these will improve performance. - Some lighter weight operating systems use fewer system resources allowing the system to devote more to running the user's applications. - A fragmented HDD runs slowly as time is spent finding parts of the files. This is reduced by defragmenting and storing the parts of the file contiguously. - Malware can slow down a computer. Removing it will improve performance. **AO3.3: Evaluation** The following is indicative of possible evaluation points that candidates may refer to but is not prescriptive or exhaustive: Hardware improvements (i.e. CPU, RAM, secondary storage and GPU) have costs attached but likely to have most impact. The higher performance the hardware, the more cost incurred. (NB candidates aren't expected to know relative costs of components.) GPU unlikely to benefit student in this scenario (unless their course requires graphics processing).

Question			Answer/Indicative content	Marks	Guidance
					Defragmenting HDD is free and so should be performed. Running anti-malware programs is free/low cost and should be done as a precaution against losing data anyway. Moving to lighter weight software can potentially be free if the user considers open source software. **Examiner's Comment** Candidates were assessed on the quality of their extended response in this question. Most candidates could cite some methods for improving performance but not all managed to then appropriately apply these to the question. Many candidates did recommend one or more measures although some cases needed to include justification. This resulted in some very good responses and marks awarded spanning the range of marks available.
			Total	9	