AQA Computer Science A-Level

4.7.1 Internal hardware components of a computer

Past Paper Mark Schemes

Additional Specimen Paper 2

04	**1**	**Mark is for AO1 (understanding)** Architecture A;	1

04	**2**	**1 mark for AO1 (recall): Situation (MAX 1 mark):** Digital signal processing; Microprocessors / embedded devices / microcontrollers; **A.** Internal processor structure for caching **A.** other reasonable examples **2 marks for AO1 (understanding): Advantages (MAX 2 marks):** Instruction and data can be accessed simultaneously; Avoid/reduce bottleneck of single data/address bus(es) // avoid/reduce delays waiting for memory fetches; Instruction and data memory can have different word lengths; Different technologies can be used to implement instruction and data memory; Different quantities of instruction and data memory means that address lengths can differ between the two // memory address structures can differ; Avoids possibility of data being executed as code, which is one method that can be exploited by hackers;	3

January 2010 Comp 2

3	(a)		Program Counter; **A** Sequence Control Register **R** Next Instruction Register Current Instruction Register; **A** Instruction Register Memory Buffer Register; **A** Memory Data Register Memory Address Register; **MAX 2**	2

3	(b)		Address in MAR/address to fetch instruction from, sent down Address Bus to Main Memory; **R** address in PC (program counter) Contents of address accessed in Main Memory; **A** by implication if contents of address location referred to during data transfer Contents of address location//instruction//data passed down Data Bus into MBR/to processor; **A** MDR instead of MBR **A** RAM for Main Memory **MAX 2**	2

3	(c)		Order of execution unimportant/one step does not rely on prior completion of the other; Steps carried out by different (hardware) devices/components; **A** operations are independent **A** operations use different registers **R** using different buses **MAX 1**	1

January 2011 Comp 2

1	a		Address (bus);	1	

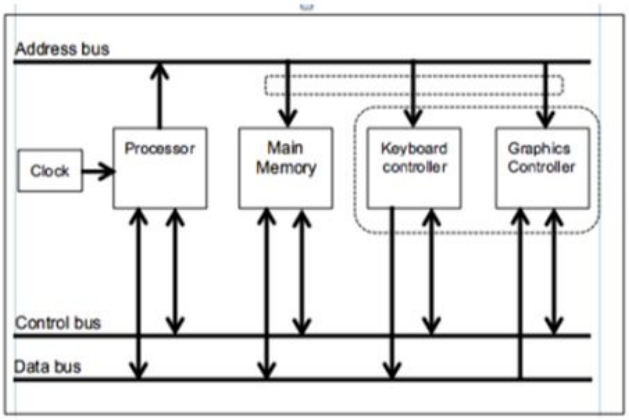
1	b		1; **R** 33	1	

1	c		A – Visual display unit; **A** VDU B – Processor; **R** CPU C – (Main) memory; D – Keyboard;	4	

January 2013 Comp 2

2	**a**		A set of/group of/parallel wires/lines; that are used to connect together components (inside the computer) // connect different parts of the CPU; in order to pass signals between them; **R** a wire **A.** connect different parts of the computer **NE** data	**MAX 2**	Wires needs to be qualified with set/group

2	**b**		Instructions; **A.** Commands / machine-code **R** signals ***Examples of a control signal (max 1):*** Clock/timing; reset; interrupt ACK; interrupt request; bus grant; bus request; status; I/O write; I/O read; memory read; memory write; transfer ACK **A.** interrupt **A.** transfer request **A.** read/write **NE** load /store **NE** clock speed	**2**	**NE** an event that details when an interrupt would be caused

2	**c**		 1 mark – one of processor, keyboard controller or graphics controller identified correctly 2 marks – all three correctly identified Address bus connects the 4 components; Arrow from processor to the address bus; Arrows from address bus to the three other components;	**5**	Mark this on where the candidate has put the components.

June 2011 Comp 2

7	**a**		1 – clock; 2 – (Main) memory / IAS ; **A** RAM **R** ROM 3 – Control bus; 4 – VDU controller / output controller; **A** controller for other named output device 5 – Processor ; **R** Central Processing Unit / CPU	**5**

7	**d**		Address bus has 64 lines / tracks/ wires // there are 2 ^64 memory locations available; **NE** 64 bits wide, moves 64 bits of data	**1**

June 2017 AS Paper 2

06	1	**Marks are for AO1 (understanding)** Harvard uses separate memory/bus/address space // von Neumann uses combined memory/bus/address space; for instructions/program and data; **NE.** Places, locations, registers, areas of memory **A.** Main memory **NOTE:** It must be clear that instructions/data are stored in separate memory, not separately in memory.	**2**

06	2	**Mark is for AO1 (knowledge)** Harvard; **R.** more than one lozenge shaded	**1**

06	3	**2 marks for AO1 (knowledge) and 4 marks for AO1 (understanding)** **Level of response question** **Level / Description / Mark Range** 3 / At least five of the steps of the cycle have been correctly identified in order/the steps are all in correct order and covering all three of the stages (fetch, decode, execute). For the top mark in this level thorough understanding of how the cycle works is evident. / 5-6 2 / At least three steps of the cycle have been identified in order, covering at least two of the stages (fetch, decode, execute). Some understanding of how the cycle works is evident. / 3-4 1 / At least one step of the cycle have been identified, covering at least one stage (fetch, decode or execute). The order of the steps may not be correct. Little understanding of how the cycle works is evident. / 1-2 **Points may include:** **Fetch:** Contents of Program Counter / PC transferred to Memory Address Register / MAR Address bus used to transfer this address to main memory Transfer of content uses the data bus Contents of addressed memory location loaded into the Memory Buffer Register / MBR Increment (contents of) Program Counter / PC **A**. at any part of fetch process after transferring PC to MAR Increment Program Counter / PC and fetch simultaneously Contents of MBR copied to CIR **Decode:** Decode instruction held by the (Current) Instruction Register / (C)IR The control unit decodes the instruction Instruction split into opcode and operand **Execute:** If necessary, data is fetched If necessary, data is stored in memory The opcode identifies the type of operation/instruction to be performed (by the processor) Result (may be) stored in register/accumulator The operation (identified by the opcode) is performed by the processor. **A.** ALU Status register updated If jump / branch required Program Counter/PC is updated **NE.** Register notation **A.** Memory Data Register/MDR for Memory Buffer Register/MBR **I.** Incorrect headings	6

June 2017 Paper 2

01	3	**All marks AO1 (understanding)** Instruction and data can be accessed simultaneously; Avoid/reduce bottleneck of single data/address bus(es) // avoid/reduce delays waiting for memory fetches; Avoids possibility of data being executed as code (which is one method that can be exploited by hackers); Being able to use exclusively ROM for instruction memory prevents the program being modified/hacked; **A.** Program cannot be accidentally overwritten (by data) Instruction and data memory can have different word lengths; Different technologies can be used to implement instruction and data memory; Different quantities of instruction and data memory means that address lengths can differ between the two // memory address structures can differ; **MAX 2** **NE.** So programs/tasks will run faster **NE.** More efficient	**2**

June 2009 Comp 2

6					
	Internal Components		**Peripherals**		
	Data Bus	10	*Keyboard*	2	
	Address Bus	9	*Visual Display Unit*	3	
	Control Bus	NA	Secondary Storage	NA	
	VDU Controller	8			
	Disk Controller	NA			
	Keyboard Controller	7			
	Main Memory	5			
	Processor	4			
	1 mark for each correct answer (10,9,5,4) **1 mark for correct pair (8,3)** **1 mark for correct pair (7,2)** **MARK DIAGRAM IF ANSWERS WRITTEN ON IT INSTEAD OF IN TABLES. ANSWERS IN TABLES OVERRIDE ANSWERS ON DIAGRAM.**				**6**

Specimen Paper 2

1		**All marks AO1 (understanding)** **1 mark** per correct answer **A.** If same response used more than once	4

	Correct Name from List
B	Visual display unit;
C	Processor;
D	Main memory;
E	Keyboard;