

# OCR Computer Science A Level

## 1.1.2 Types of Processor

### Intermediate Notes



**Specification:**

**1.1.2 a)**

- RISC Processors
- CISC Processors
- The difference between RISC and CISC

**1.1.2 b)**

- GPUs and their uses

**1.1.2 c)**

- Multicore Systems
- Parallel Systems



## RISC and CISC processors

### Reduced Instruction Set Computers (RISC)

In these processors, there is a **small instruction set**. Each instruction is approximately **one line of machine code** and takes one clock cycle.

### Complex Instruction Set Computers (CISC)

In these processors there is a **large instruction set**. The aim is to try and accomplish tasks in as few lines of assembly code as possible. These instructions are built into the **hardware**. Early on these processors were used as the standard, however with time they got replaced by RISC design. Now they are used more in **microcontrollers** and **embedded systems**.

### Comparison between RISC and CISC

RISC Processors	CISC Processors
The compiler has to do more work to translate high level code into machine code.	The compiler has less work to translate high level code into machine code.
More RAM is required to store the code.	Less RAM is required since code is shorter.
Pipelining is possible since each instruction takes one clock cycle.	Many specialised instructions are made, even though only a few of them are used.

*A-Level only*

### **Graphics Processing Unit (GPU)**

A graphics processing unit (GPU) is a **co-processor** which has lots of **independent processors** working in parallel making it very efficient at tasks such as image processing, and machine learning.

### **Multi-core and Parallel Systems**

Multi-core CPUs have **multiple independent cores** that can complete instructions separately which results in higher performance. Parallel systems accomplish a similar task however instead of requiring multiple cores they can complete tasks with a single core, by using **threading**. Overall, in larger projects, multi-core systems perform better than parallel systems.



