# AQA Computer Science A-Level

## 4.7.3 Structure and role of the processor and its components

Concise Notes

**Specification:**

**4.7.3.1 The processor and its components:**

Explain the role and operation of a processor and its major components:

- arithmetic logic unit
- control unit
- clock
- general-purpose registers
- dedicated registers, including:
    - program counter
    - current instruction register
    - memory address register
    - memory buffer register
    - status register

**4.7.3.2 The Fetch-Execute cycle and the role of registers within it:**

Explain how the Fetch-Execute cycle is used to execute machine code programs including the stages in the cycle (fetch, decode, execute) and details of registers used.

**4.7.3.3 The processor instruction set:**

Understand the term ‘processor instruction set’ and know that an instruction set is processor specific.

Know that instructions consist of an opcode and one or more operands (value, memory address or register).

**4.7.3.4 Addressing modes:**

Understand and apply immediate and direct addressing modes.

### 4.7.3.5 Machine-code/assembly language operations:

Understand and apply the basic machine-code operations of:

- load
- add
- subtract
- store
- branching (conditional and unconditional)
- compare
- logical bitwise operators (AND, OR, NOT, XOR)
- logical
    - shift right
    - shift left
- halt

Use the basic machine-code operations above when machine-code instructions are expressed in mnemonic form- assembly language, using immediate and direct addressing.

### 4.7.3.6 Interrupts:

Describe the role of interrupts and interrupt service routines (ISRs); their effect on the Fetch-Execute cycle; and the need to save the volatile environment while the interrupt is being serviced.

### 4.7.3.7 Factors affecting processor performance:

Explain the effect on processor performance of:

- multiple cores
- cache memory
- clock speed
- word length
- address bus width
- data bus width

## The processor and its components

- Every computer contains a processor which executes instructions in order to run programs
- Processors contain:
  - an arithmetic logic unit (ALU)
  - a control unit
  - numerous registers

### Arithmetic logic unit (ALU)

- Performs arithmetic and logic operations
- Arithmetic operations are mathematical operations like addition
- Logic operations include AND, OR and XOR

### Control unit

- Responsible for controlling the various components of the processor
- Controls the fetch-execute cycle

### Registers

- Small storage locations used to hold data temporarily
- Have high read and write speeds
- General purpose registers can be used as storage for any data that is required by instructions during execution
- Special purpose registers are assigned to the storage of specific information

| Special purpose register | Purpose |
|---|---|
| Program counter (PC) | ● Holds the memory address of the next instruction to be executed in the fetch-execute cycle |
| Current instruction register (CIR) | ● Holds the instruction that is currently being executed by the processor |
| Memory address register (MAR) | ● Stores the memory address of a memory location that is to be read from or written to |
| Memory buffer register (MBR) | ● Also called the memory data register (MDR)<br>● Holds the contents of a memory location that has been read from or data that is to be stored |
| Status register (SR) | ● Contains a number of bits, the values of which can change to indicate the occurrence of an interrupt |

<u>Clock</u>

- Found in a computer's processor
- Generates a timing signal which changes at a regular frequency
- Used to synchronise communication between the components of the processor and the rest of the computer system

## The Fetch-Execute cycle

- A continuous cycle performed by the processor
- Consists of three stages:
  - Fetch
  - Decode
  - Execute

<u>Fetch</u>

The next instruction to execute is retrieved from main memory

1. The content of the PC is copied to the MAR
2. The content of the MAR is transferred to main memory by the address bus
3. The instruction is sent from main memory to the MBR by the data bus
4. The PC is incremented by one
5. The content of the MBR is copied to the CIR

<u>Decode</u>

The fetched instruction is decoded

1. The content of the CIR is decoded by the control unit
2. The decoded instruction is split into two parts: opcode and operands

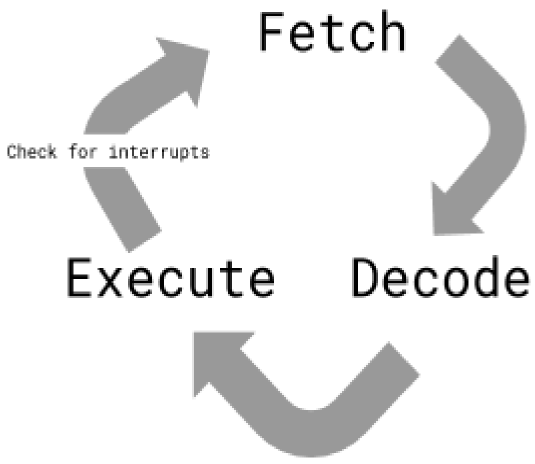
<u>Execute</u>

The instruction is carried out

1. Any data required by the instruction that isn't present in registers is fetched
2. The instruction is carried out
3. Results of any calculations are stored in general purpose registers or main memory

<u>Check for interrupts</u>

- Between each execute stage and fetch stage of the cycle
- The content of the status register is checked for changes
- Any changes could signify the occurrence of an interrupt



## The processor instruction set

- The group of instructions that a processor can carry out
- Each type of processor has its own instruction set
- Instructions for one processor may not be compatible with other processors
- Instructions are usually stored in machine code and consist of two primary parts:
    - opcode
    - one or more operands
- Opcode specifies the type of operation that is to be carried out
- Operands are the pieces of data on which the operation is performed

Addressing modes

- One bit in a machine code instruction is usually assigned to the addressing mode in use
- There are two addressing modes:
    - Immediate - The value specified in the operand is to be treated as the actual value to be used in an operation
    - Direct - The value specified by an operand signifies a memory address

## Machine-code/assembly language operations

- The table below lists the basic machine-code operations and their equivalent in AQA's assembly language
- This will be used in exam questions
- You need to learn to both interpret and write AQA assembly language

| Operation | AQA Assembly Language | Description |
|---|---|---|
| **Load** | `LDR Rx, <memory reference>` | Load the value stored in the memory location specified by `<memory reference>` into register x. |
| **Store** | `STR Rx, <memory reference>` | Store the value that is in register x into the memory location specified by `<memory reference>`. |
| **Add** | `ADD Rx, Ry, <operand>` | Add the value specified by `<operand>` to register y and store the result in register x |

| | | |
|---|---|---|
| **Subtract** | `SUB Rx, Ry, <operand>` | Subtract the value specified by `<operand>` from the value in register y and store the result in register x. |
| **Move** | `MOV Rx, <operand>` | Copy the value specified by `<operand>` into register x. |
| **Compare** | `CMP Rx, <operand>` | Compare the value stored in register x with the value specified by `<operand>`. |
| **Branch (unconditional)** | `B <label>` | Always branch to the instruction at the position specified by `<label>` in the program. |
| **Branch (conditional)** | `B<condition> <label>` | Branch to the instruction at position `<label>` if the last comparison met the criterion specified by `<condition>`.<br><br>Possible values for `<condition>` are:<br><br>● EQ: equal to<br>● NE: not equal to<br>● GT: greater than<br>● LT: less than |
| **Logical AND** | `AND Rx, Ry, <operand>` | Perform a bitwise logical AND operation between the value in register y and the value specified by `<operand>` and store the result in register x. |
| **Logical OR** | `ORR Rx, Ry, <operand>` | Perform a bitwise logical OR operation between the value in register y and the value specified by `<operand>` and store the result in register x. |
| **Logical XOR** | `EOR Rx, Ry, <operand>` | Perform a bitwise logical XOR (exclusive or) operation between the value in register y and the value specified by `<operand>` and store the result in register x. |

| | | |
|---|---|---|
| **Logical NOT** | `MVN Rx, <operand>` | Perform a bitwise logical NOT operation on the value specified by `<operand>` and store the result in register x. |
| **Logical shift left** | `LSL Rx, Ry, <operand>` | Logically shift left the value stored in register y by the number of bits specified by `<operand>` and store the result in register x. |
| **Logical shift right** | `LSR Rx, Ry, <operand>` | Logically shift right the value stored in register y by the number of bits specified by `<operand>` and store the result in register x. |
| **Halt** | `HALT` | Stops the execution of the program |

Logical shift

- An operation that can be performed on binary numbers
- Involves shifting all of the bits in a number a specified number of positions to the right or to the left
- The result is a number that has been doubled or halved a specified number of times

## Interrupts

- Signals sent to the processor by another part of the computer requesting the attention of the processor
- Both hardware and software can also send interrupts
- Detected as a change in the content of the status register between the execute and fetch stages of the fetch-execute cycle
- Can be handled using the vectored interrupt method:
    - When an interrupt occurs, the processor stops executing the current program and places the content of its registers onto the system stack
    - The processor loads the appropriate interrupt service routine: a series of instructions for handling the interrupt that is specific to the type of interrupt
    - Once the interrupt service routine is finished, the processor restores the volatile environment from the system stack and resumes execution of any programs that were running before the interrupt

## Factors affecting processor performance

- A processor's performance is key to the speed of a computer
- There are numerous factors that can affect a processor's performance

Number of cores

- The number of cores a processor has directly affects the performance of the processor
- Each core can perform its own fetch-execute cycle independently of others
- Different applications can be allocated different cores

Cache memory

- A small portion of incredibly fast memory
- Has read and write speeds far higher than hard disk drives and even SSDs
- Used to store frequently used information and reduces time wasted in fetching the same information from main memory time and time again
- The more cache a processor has, the more information it can store and the more time it can save in fetching information from main memory

Clock speed

- Relates to the frequency of the pulses generated by the system clock
- The higher the frequency, the more cycles of the fetch-execute cycle can be completed in the same period of time
- Errors can occur when a computer's clock speed is increased too far

Word length

- A word is a group of bits that is treated as a single unit by a processor
- Words can be used for representing both instructions and data
- The length of a word is the number of bits that are assigned to it
- Higher word lengths allow for more bits to be transferred and manipulated as a single unit

Address bus width

- The width of a bus relates to the number of parallel wires that make up the bus
- Increasing the width of the address bus increases the range of addresses that it can specify
- Increasing the width of the address bus increases the computer's amount of addressable memory
- Adding a single wire doubles the number of addressable memory locations

Data bus width

- Increasing the width of the data bus increases the volume of data that can be transferred over the bus at any one time
- A wider data bus allows the processor to fetch more data from main memory in one cycle of the fetch-execute cycle
- This reduces the number of cycles required to fetch large volumes of data